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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,383	04/19/2000	Stephen L. Willis	MICRON.092CP1	3147

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/552,383	WILLIS, STEPHEN L.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-37 and 56-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-37 and 56-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 26, 2004 has been entered.

Terminal Disclaimer

The terminal disclaimer filed on February 26, 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Pat. No. 6,576,553 B2 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 30-37 and 56-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al. (US 6,268,291 B1) in view of Sandhu et al. (US Pat. No. 5,069,002).

Claims 30-32, 34 and 56-58, Andricacos et al. teaches a method comprising the steps of: forming a dielectric layer (the layer formed between stop layers 92 in figs. 4A and 5A, similar to the layer 54 in figure 2) of a first thickness on a semiconductor wafer (52) (see Fig. 2); forming an aperture in the dielectric layer (see opening) (see figs. 4A and 5A); positioning a shield layer (92) (see figs. 4A and 5A) of a material different than the dielectric layer (see col. 8, lines 31-34 and 37-38, col. 9, lines 50-54; and col. 10, lines 17-18); positioning a sacrificial layer (94) (see figs. 4A and 5A); depositing conductive material (90 and 100) (see figs. 4A and 5A); removing the conductive material and the sacrificial layer using a CMP process (see figs. 4B and 5B and col. 10, lines 21-22 and 30-31) adapted to remove the conductive material (90 and 100) and the sacrificial layer (94) until the shield layer (92) is reached (see figs. 4B and 5B), wherein the shield layer (92) is more resistant to planarization by the CMP process than the sacrificial layer (94) (please note that the shield layer 92, contrary to the sacrificial layer 94, remains after the planarization step, see figs. 4B and 5B), and wherein the shield layer (92) inhibits thinning of the dielectric layer (the layer between the stop layers 92) during the CMP process (please note that the planarization is stopped when the shield layer 92 is exposed, see figs. 4B and 5B), and wherein interposing the sacrificial layer (94) between the conductive material (90 and 100) and the shield layer (92) reduces the amount of conductive material on the shield layer following the CMP process (see figs.

4B and 5B). Furthermore, Andricacos et al. teaches halting the CMP process when the sacrificial layer (94) has been removed (see figs. 4B and 5B) so as to maintain the dielectric layer (the layer between the stop layers 92) at the first thickness (please note that the shield layer 92 protects the dielectric layers from the effect of the planarization step, see figs. 4B and 5B).

However, Andricacos et al. is silence with respect to the limitation of detecting when the CMP process has removed the sacrificial layer. Sandhu et al. teach that is well known in the art to perform a sensing step during the CMP process, in which the change in friction is detected by rotating the wafer and polishing surfaces with electric motors and measuring current changes on one or both of the motors (see abstract and col. 3, lines 38-41 and 55-63 and col. 4, lines 28-30).

Andricacos et al. and Sandhu et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include the step of detecting when the CMP process has removed the sacrificial layer. The motivation for doing so, as is taught by Sandhu et al., is providing a control means for adjusting or stopping the process (abstract). Therefore, it would have been obvious to combine Sandhu et al. with Andricacos et al. to obtain the invention of claims 30-37 and 56-62.

Regarding claims 33, 36, 59 and 61, Andricacos et al. teaches that it is very well known in the art to select an oxide material for the dielectric and/or the sacrificial layers, and a nitride material for the shield layer (see col. 8, lines 31-34, 37-38 and 51-53, col. 9, lines 50-54; and col. 10, lines 17-18), and hence, the use of the claimed particular

materials (i.e. BPSG and oxynitride (DARC)) to make the dielectric, shield and sacrificial layers, absent any criticality, are only considered to be the use of "optimum" or "preferred" materials that a person having ordinary skill in the art at the time the invention was made using routine experimentation would have found obvious to provide for the dielectric, shield and sacrificial layers in the device disclosed by Andricacos et al. since they are well known types of materials used to make such layers and since it has been held to be a matter of obvious design choice and within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use of the invention. In re Leshin, 125 USPQ 416.

Regarding claims 35 and 60, Andricacos et al. teaches that the shield layer (92) is comprised of silicon nitride (see col. 10, lines 17-18 and 26-27).

Regarding claims 37 and 62, Denning et al. teaches a cavity (consider the damascene structure) filled with the conductive material (90 or 100) (see figs. 4B and 5B).

Response to Arguments

Applicant's arguments with respect to claims 30-37 and 56-62 have been considered but are moot in view of the new ground of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
3/18/04

Tom Thomas
Tom Thomas
Supervisory Patent
Technology